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Date: 7/5/06

Patent No. : 7,033,895 B2
ApplicationNo.: 10/823,420
Issued : April 25, 2006
Inventor : Lee, et al.
Title : METHOD OF FABRICATING A MOS TRANSISTOR WITH ELEVATED SOURCE/DRAIN STRUCTURE USING A SELECTIVE EPITAXIAL GROWTH PROCESS
Docket No:

Re: Request for Certificate of Correction

Consideration has been given your request for the issuance of a certificate of correction, for the above-identified patent under the provision of Rule 1.322 or 1.323.

Respecting the alleged errors, in columns 7 and 8, lines 16 and 17, is an editing change made in accordance with the style of the Invention Patent Manual. Therefore, no correction(s) is in order here under United States Codes (U.S.C.) 254 or 255 the Code of Federal Regulation (C.F.R.) R 1.322 R 1.323.

In view of the foregoing, your request in these matters is hereby denied.

A certificate of correction will be issued to correct the remaining errors noted in your request.

Further correspondence concerning this matter should be filed and directed to Decisions and Certificates of Correction Branch. Any response must be filed within a four week period.

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